IFW

Patent

Docket No.: TRAN-P283

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.					
Date of Deposit:	03/15/05	Name of Person Making the Deposit:	Donna Petford	Signature of the Person Making the Deposit:	Donna Petford

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Eric Chen-Li SHENG, David HOFFMAN, John Laurence NIVEN

Application No.: 10/791,099 Group Art Unit:

Filed: 03/01/04 Examiner:

Title: SYSTEM AND METHOD FOR REDUCING TEMPERATURE VARIATION DURING BURN-IN

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
_X_ Information Disclosure statement (_2_ sheets)
..... Information Disclosure statement and late filing fee
_X_ Form 1449
..... Petition for Extension of Time
..... Other: .....

Fee Calculation (for other than a small entity)

Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	0.00
Information Disclosure Statement, late filing				$180.00	0.00
Other:					
Total Fees					0.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060
Customer No: 000041066

Respectfully submitted,

Date: 3/15/2005

By: _____
Anthony C. Murabito
Reg. No. 35,295

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P283

Inventor(s): Eric Chen-Li SHENG, David HOFFMAN, John Laurence NIVEN

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P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,119,337	SEMICONDUCTOR MEMORY DEVICE HAVING BURN-IN TEST FUNCTION	06/02/92
5,406,212	BURN-IN APPARATUS AND METHOD FOR SELF-HEATING SEMICONDUCTOR DEVICES HAVING BUILT-IN TEMPERATURE SENSORS	04/11/95
5,844,429	BURN-IN SENSING CIRCUIT	12/01/98
6,037,792	BURN-IN STRESS TEST MODE	03/14/00
6,100,751	FORWARD BODY BIASED FIELD EFFECT TRANSISTOR PROVIDING DECOUPLING CAPACITANCE	08/08/00
6,104,061	MEMORY CELL WITH VERTICAL TRANSISTOR AND BURIED WORD AND BODY LINES	08/15/00
6,114,866	SEMICONDUCTOR DEVICE TEST BOARD AND METHOD FOR EVALUATING SEMICONDUCTOR DEVICES	09/05/00
6,157,201	BURN-IN SYSTEM FOR RELIABLE INTEGRATED CIRCUIT MANUFACTURING	12/05/00
6,137,301	EPROM USED AS A VOLTAGE MONITOR FOR SEMICONDUCTOR BUR-IN	10/24/00

6,218,892	DIFFERENTIAL CIRCUITS EMPLOYING FORWARD BODY BIAS	04/17/01
6,262,588	BIAS MONITOR FOR SEMICONDUCTOR BURN-IN	07/17/01
6,310,485	INTEGRATED CIRCUIT DEVICE HAVING A BURN-IN MODE FOR WHICH ENTRY INTO AND EXIT FROM CAN BE CONTROLLED	10/30/01

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Attorney Docket No.: TRAN-P283

Inventor(s): Eric Chen-Li SHENG, David HOFFMAN, John Laurence NIVEN

Application No.: 10/791,099 Group Art Unit:

Filed: 03/01/04 Examiner:

Title: SYSTEM AND METHOD FOR REDUCING TEMPERATURE VARIATION DURING BURN-IN

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5,119,337	06/02/92	Shimizu et al.	365	201	04/16/90
	B	5,406,212	04/11/95	Hashinaga et al.	324	760	07/17/92
	C	5,844,429	12/1/98	Cho	327	68	07/15/96
	D	6,037,792	03/14/00	McClure	324	760	12/21/96
	E	6,100,751	08/08/00	De et al.	327	534	05/13/98
	F	6,104,061	08/15/00	Forbes et al.	257	330	02/27/98
	G	6,114,866	09/05/00	Matsuo et al.	324	760	02/04/98
	H	6,157,201	12/05/00	Leung, Jr.	324	760	01/28/98
	I	6,137,301	10/24/00	Chen	324	760	05/11/98
	J	6,218,892	04/17/01	Soumyanath et al.	327	537	02/24/99
	K	6,262,588	07/17/01	Chen	324	765	08/07/00
	L	6,310,485	10/30/01	McClure	324	760	01/27/00
	M						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	N							
	O							
	P							
	Q							
	R							
	S							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	T	

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.